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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,079	09/10/2003	Dale John Shidla	200310484-1	2735

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EXAMINER	
ASSESSOR, BRIAN J	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,079	SHIDLA ET AL.	
	Examiner	Art Unit	
	Brian J. Assessor	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/10/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/31/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 18 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 2005/0055683 A1. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 1 of Application No. 2005/0055683 A1 contains every element of claim 18 of the instant application and thus anticipate the claim of the instant application. Claim 18 of the instant application therefore is not patently distinct from the earlier patent claim and as such is unpatentable over obvious-type double patenting. A later application

claim is not patentably distinct from an earlier claim if the later claim is not anticipated by the earlier claim.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 18 and 19 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The program product needs to be stored on the computer readable medium in order to be acceptable under 35 USC 101.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 10-14, 16, 17, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Quach (6,640,313).

As per claim 1, Quach teaches:

A method of providing CPU functional testing, the method comprising:

executing operations on multiple functional units of a same type in the CPU; (Quach column 6, lines 1-2)

automatically comparing outputs from the multiple functional units; and checking results of the comparison only for redundant operations. (Quach column 6, lines 5-7)

As per claim 2, Quach teaches:

The method of claim 1, wherein automatically comparing the outputs from the multiple functional units is performed by comparator circuitry within the CPU that is coupled to receive the outputs. (Quach column 6, lines 1-2)

As per claim 3, Quach teaches:

The method of claim 2, further comprising: setting a comparison flag based on output of the comparator circuitry. (Quach column 7, line 66 – column 6, line 2)

As per claim 4, Quach teaches:

The method of claim 3, wherein checking results of the comparison is performed by examining the comparison flag. (Quach column 7, line 66 – column 6, line 2)

As per claim 5, Quach teaches:

The method of claim 4, further comprising: if examination of the comparison flag indicates an error, then halting the execution and providing a

notification of the error. (Quach column 7, line 66 – column 6, line 8; when there is an error signal when the comparator does not match.)

As per claim 10, Quach teaches:

The method of claim 1, wherein the functional units comprise floating point units. (Quach figure 1, element 158)

As per claim 11, Quach teaches:

The method of claim 1, wherein the functional units comprise arithmetic logic units. (Quach figure 1, element 154)

As per claim 12, Quach teaches:

A microprocessor with built-in functional testing capability, the microprocessor comprising:

multiple functional units of a same type; (Quach column 6, lines 1-2)

registers that receive outputs from the multiple functional units; (inherent; in all processing systems each functional unit has a register to store the result of the computation.)

comparator circuitry that also receives the outputs from the multiple functional units and compares the outputs to provide functional testing. (Quach column 6, lines 5-7)

As per claim 13, Quach teaches:

The microprocessor of claim 12, wherein the multiple functional units comprise floating point units. (Quach figure 1, element 158)

As per claim 14, Quach teaches:

The microprocessor of claim 12, wherein the multiple functional units comprise arithmetic logic units. (Quach figure 1, element 154)

As per claim 16, Quach teaches:

The microprocessor of claim 12, further comprising: at least one flag coupled to receive results from the comparator circuitry. (Quach column 7, line 66 – column 6, line 2)

As per claim 17, Quach teaches:

The microprocessor of claim 16, wherein the flag is ignored if different operations are performed on the multiple functional units and is checked if a same redundant operation is performed on the multiple functional units. (Quach column 7, line 66 – column 6, line 8; when there is no error signal when the comparator matches.)

As per claim 20, Quach teaches:

A apparatus for providing CPU functional testing, the apparatus comprising:

means for executing operations on multiple functional units of a same type in the CPU; (Quach column 6, lines 1-2)

means for automatically comparing outputs from the multiple functional units; (Quach column 6, lines 5-7)

means for checking results of the comparison only for redundant operations. (Quach column 6, lines 5-7)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9, 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach (6,640,313) in view of Fruehling (6,625,688).

As per claim 6:

Quach fails to explicitly disclose a method wherein the redundant operations are opportunistically scheduled by a compiler to take advantage of an otherwise idle functional unit during a cycle.

In column 11, lines 32-34; Fruehling clearly teaches a method for taking advantage of idle CPU cycles. The parallel signature analyzer (PAS) uses the idle cycles to compare CPU signals and to monitor the health of the CPU.

It would have been obvious to a person of ordinary skill in the art at the time of invention to include the opportunistic behavior as taught by Fruehling to take advantage of idle and unused processing cycles. This would have been obvious because Fruehling clearly teaches that the above method is a more time effective and a better method for testing a CPU, with hurting processing throughput. (Fruehling coulumn 5, lines 30-40)

As per claim 7:

The method of claim 6, wherein the compiler is configured with various levels of aggressiveness with respect to scheduling of the redundant operations. (Fruehling column 11, lines 47-48)

As per claim 8:

The method of claim 7, wherein the levels of aggressiveness include levels more aggressive than just taking advantage of otherwise idle functional units. (Fruehling column 12, lines 60-65; the system can be configured to force the CPU to go idle.)

As per claim 9:

The method of claim 8, wherein a high level of aggressiveness forces all operations on a functional unit to be performed redundantly on another functional unit of the same type. (Fruehling column 12, lines 60-65; the system can be configured to force the CPU to go idle.)

As per claim 15:

Quach fails to explicitly disclose a method wherein the microprocessor executes a program which is compiled by a compiler that opportunistically schedules redundant operations to take advantage of an otherwise idle functional unit during a cycle.

In column 11, lines 32-34; Fruehling clearly teaches a method for taking advantage of idle CPU cycles. The parallel signature analyzer (PAS) uses the idle cycles to compare CPU signals and to monitor the health of the CPU.

It would have been obvious to a person of ordinary skill in the art at the time of invention to include the opportunistic behavior as taught by Fruehling to take advantage of idle and unused processing cycles. This would have been obvious because Fruehling clearly teaches that the above method is a more time effective and a better method for testing a CPU, with hurting processing throughput. (Fruehling coulumn 5, lines 30-40)

As per claim 18, Quach teaches:

A computer-readable program product for execution on a target microprocessor with multiple functional units of a same type, the program product comprising

executable code that includes a redundant operation scheduled on two functional units (Quach column 6, lines 1-7)

Quach fails to explicitly disclose a method to take advantage of one of the functional units that would otherwise be idle during a cycle.

In column 11, lines 32-34; Fruehling clearly teaches a method for taking advantage of idle CPU cycles. The parallel signature analyzer (PAS) uses the idle cycles to compare CPU signals and to monitor the health of the CPU.

It would have been obvious to a person of ordinary skill in the art at the time of invention to include the opportunistic behavior as taught by Fruehling to take advantage of idle and unused processing cycles. This would have been obvious because Fruehling clearly teaches that the above method is a more time effective and a better method for testing a CPU, with hurting processing throughput. (Fruehling coulumn 5, lines 30-40)

As per claim 19, Quach teaches:

The program product of claim 18, wherein the program product is configured to execute on a microprocessor having comparator circuitry to automatically compare outputs of the two functional units. (Quach column 6, lines 1-7)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Assessor whose telephone number is (571) 272-0825. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BA

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER